Claims

[c1] 1. A method for fabricating a Mask ROM, comprises:
forming a plurality of buried bit lines in a substrate;
forming a gate dielectric layer on the substrate;
forming a conductive layer on the substrate;
forming a first blocking layer on the conductive layer;
patterning the first blocking layer and the conductive layer into a plurality of first blocking strips and a plurality of word lines, respectively;
forming a plurality of second blocking strips between the word lines and between the first blocking strips;
forming a first patterned photoresist layer on the substrate covering the buried bit lines;
removing a portion of the first blocking strips to form a plurality of blocking bumps by using the first patterned photoresist layer as a mask, wherein the blocking bumps and the second blocking strips together define a plurality of pre-coding windows;
removing the first patterned photoresist layer;
forming a second patterned photoresist layer having a plurality of coding windows therein on the substrate, wherein the coding windows expose selected pre-coding windows and a coding window is larger than a pre-coding window;
performing a coding implantation to form a plurality of implanted coding regions under the selected pre-coding windows exposed by the coding windows with the second patterned photoresist layer, the blocking bumps and the second blocking strips as mask; and
removing the second patterned photoresist layer.

[c2] 2. The method of claim 1, wherein the first blocking layer comprises polysilicon.

[c3] 3. The method of claim 1, further comprising forming an isolating layer on the conductive layer before the first blocking layer is formed.

[c4] 4. The method of claim 3, wherein the isolating layer comprises silicon oxide.

[c5] 5. The method of claim 1, wherein an etching rate of the second blocking strips is lower than that of the first blocking strips during removing a portion of the

first blocking strips to form the blocking bumps.

[c6] 6. The method of claim 1, wherein the gate dielectric layer comprises a gate oxide layer.

[c7] 7. The method of claim 1, wherein forming a plurality of second blocking strips between the word lines and between the first blocking strips comprises:
forming a second blocking layer on the substrate filling gaps between the word lines and between the first blocking strips; and
removing a portion of the second blocking layer until tops of the first blocking strips are exposed.

[c8] 8. The method of claim 7, wherein removing a portion of the second blocking layer comprises performing chemical mechanical polishing (CMP).

[c9] 9. The method of claim 7, wherein removing a portion of the second blocking layer comprises performing etching-back.

[c10] 10. A method for fabricating a Mask ROM, comprises:
forming a plurality of buried bit lines in a substrate;
forming a plurality of word lines and a plurality of first blocking strips thereon on the substrate;
forming a plurality of second blocking strips between the word lines and between the first blocking strips;
patterning the first blocking strips into a plurality of blocking bumps, wherein the blocking bumps and the second blocking strips together define a plurality of pre-coding windows;
forming a coding mask layer having a plurality of coding windows therein on the substrate, wherein the coding windows expose selected pre-coding windows;
performing a coding implantation to form a plurality of implanted coding regions under the selected pre-coding windows exposed by the coding windows; and
removing the coding mask layer.

[c11] 11. The method of claim 10, wherein forming the word lines and the first blocking strips comprises:

forming a conductive layer on the substrate;
forming a first blocking layer on the conductive layer; and
patterning the first blocking layer and the conductive layer into a plurality of first blocking strips and a plurality of word lines, respectively.

[c12] 12. The method of claim 11, wherein the first blocking layer comprises polysilicon.

[c13] 13. The method of claim 11, further comprising forming an isolating layer on the conductive layer before the first blocking layer is formed.

[c14] 14. The method of claim 13, wherein the isolating layer comprises silicon oxide.

[c15] 15. The method of claim 10, wherein an etching rate of the second blocking strips is lower than that of the first blocking strips during patterning the first blocking strips to form the blocking bumps.

[c16] 16. The method of claim 10, further comprising forming a gate dielectric layer on the substrate before the buried bit lines are formed.

[c17] 17. The method of claim 10, wherein forming a plurality of second blocking strips between the word lines and between the first blocking strips comprises:
forming a second blocking layer on the substrate filling gaps between the word lines and between the first blocking strips; and
removing a portion of the second blocking layer until tops of the first blocking strips are exposed.

[c18] 18. The method of claim 17, wherein removing a portion of the second blocking layer comprises performing chemical mechanical polishing (CMP).

[c19] 19. The method of claim 17, wherein removing a portion of the second blocking layer comprises performing etching-back.

[c20] 20. The method of claim 10, wherein the coding mask layer comprises a patterned photoresist layer.